JMN455 – SSI Design Lab II: Manufacturing Processes for Smart Systems Lab Report

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***Abstract*— USN's MST - Lab is a research laboratory cleanroom; all personnel must adhere to safety guidelines and wear proper cleanroom suits before conducting any experiments. For the SSI Design Lab II (Microfabrication) course, lab experiments were carried out encompassing six processes with sputtering, photolithography, and wet/dry etching. Three different wafers were successfully fabricated; two square structures and one to be used by BioMEMS course students. Each process was evaluated by taking measurements using a profilometer or an ellipsometer; some inconsistencies were found along the whole process during the evaluation. Such findings are discussed in this paper. The resulting wafers exhibited satisfactory properties such as expected from the entire process chain.**

Keywords—Ellipsometry, Profilometry, Photolithography, Magnetron Sputtering, Gold Etching, Reactive Ion Etching, Anisotropic Wet Etching

I. INTRODUCTION

USN's MST - Lab is certified as an ISO class 5 cleanroom, meaning there is a maximum of 3520 particles equal or larger than 0.5 microns in 1 squared meter [1, 2]. The size of the lab is 400 square meters [1]. A cleanroom suit was necessary to be worn while performing experiments in each laboratory in order to reduce particle dispersion. The suit consists of a hood, coverall, boots, gloves, face mask, and protective glasses. The hood is sometimes directly attached to the coverall.

All personnel must watch a cleanroom training video [3] showing forbidden activities and behavior in the cleanroom. Tab. 1 lists several behaviors that must be avoided in a cleanroom. The number of particles produced for one individual, in a specific activity, is shown to emphasize the contamination risk. Erroneous activities cause a particle dispersion higher than the maximum allowed for an ISO class 5 cleanroom, therefore risking contamination of cleanroom items.

TABLE I. BEHAVIORS IN A CLEANROOM [3]

Behavior or activity	**Particle production (size 0.5 microns)**
Correctly worn cleanroom garments	37 (89 when moving)
Looking at a wristwatch	8987
Unzipped coverall	12768
Eating (breaking a bisque)	18554
Reading a book	21103
Coughing without a facemask/smoking	38026
Cleaning with wiping materials that are not cleanroom compatible	40476

USN's MST- Lab has several different pieces of equipment for thin film deposition, photolithography, surface characterization, and chemical chambers for chemical mixing and wet etching. In this lab series, the AJA PVD machine, mask aligner, Spin 150 spin coater, Dektak 150 profilometer, Oxford Instruments Reactive Ion Etching chamber, and Alpha Plasma Cleaner are used. Since MST Lab is a research lab, all equipment is in the same cleanroom for convenience. However, in order to minimize contamination, it is quite common to encounter separate cleanrooms for photolithography, thin film deposition, etching, and characterization in production and industrial facilities.

Sputtering is the most important physical vapor deposition (PVD) method to grow high quality thin films. Argon (Ar) ions emitted from a glow discharge plasma hit the DC negatively biased target and eject one target atom. This ejected target atom will be transported to the wafer, this atom will hit the wafer with considerable energy [4]. Sputtering rate is determined primarily by the sputter current density and the sputter gas type, where a higher atomic mass provides higher yield. Lower gas pressure will also increase the mean free path, allowing less collision to occur between the target and substrate and improving the deposition rate [5].

Microfabrication's pattern transfer procedure is comprised of two primary steps: photolithography and etching. Photolithography is a well-tested conventional method, which main idea is to create patterns using a mask on top of a photoresist material using ultraviolet (UV) light [6]. A cleaned wafer is covered by a thin layer of photosensitive material called photoresist. In a case of positive photoresist, exposure to UV light will render the material more soluble. A chemical called developer will react with the soluble part of the photoresist and dissolve it. Next, the wafer is hard baked to stabilize the photoresist chemically and thermally for subsequent etching processes [7].

There are two types of etching techniques which may be conducted, either with dry or wet etchants, and they are referred to as dry and wet etching, respectively [4]. Compared to dry etching, wet etching is a comparatively inexpensive and easy etching procedure. In a straightforward wet etching

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setup, a heated quartz bath contains a liquid etchant, and the wafer to be etched is either sprayed or submerged in the bath.

Due to the various chemical reactions during the process, which consume the original reactants and create new ones, this liquid chemical is used to remove components off a wafer [8]. Typically, this is an acidic or basic chemical liquid, such as HF/HNO_3 HCl for a gallium arsenide (GaAs) substrate or a more concentrated acid for a silicon (Si) substrate. In most cases, basic solutions provide anisotropic outcomes, while acidic solutions are used for isotropic etching [9].

Anisotropic Si wet etching was discovered when orientation dependent behavior of some chemical solution was observed for different planes of <100>, <110>, and <111> surfaces on the silicon wafer [10]. Anisotropic etchants such as potassium hydroxide (KOH) and tetra-methyl-ammonium hydroxide (TMAH) can produce rectangular holes in <100> Si wafers as shown in Fig. 1.

Anisotropic wet etching is quite straightforward, the Si wafer is immersed in the etchant (KOH/TMAH) solution and the etching rate will be dependent on concentration, temperature, and the crystal orientation. TMAH is more commonly used in the semiconductor industry to avoid contamination from potassium [11], however KOH is cheaper and easily obtainable.

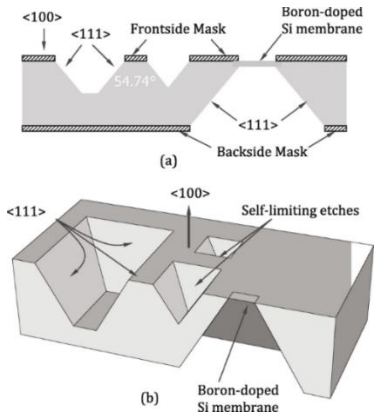


Fig. 1. Anisotropic etching profile of (100) Si wafer with self-limiting and grooved structures (a) cross-section and (b) 3D [12]

Reactive Ion Etching (RIE) is a processing technique that uses plasma for etching purposes [13]. Plasma in this context refers to gases that are subjected to specific pressure and electrical potential conditions where the gas atoms become ionized. With this it is possible to control the formation of chemically reactive species that can interact with the solid to be etched [14].

RIE process starts with a glow discharge that generates a suitable feed gas. Next, a DC bias is formed on the wafer. By convection reactive intermediates are moved from the plasma to the wafer surface. Reactive radicals are then absorbed on the wafer surface. A reaction between the absorbed species and the material to be etched takes place. When the etching is finished a desorption and exhaust process is necessary to get rid of the remaining reaction species [14].

In this paper, microfabrication processes for three different wafers spanning through six different labs are reported and discussed. Section I introduces the necessary process technology involved in wafer manufacturing in the laboratory. Section II explains each step of the fabrication process and safety practices in the cleanroom. Section III shows the measurement results and discusses the outcome of each process. Finally, conclusions related to the whole fabrication process are depicted in Section IV.

II. Methods and Fabrication Process

Three p-type (100) silicon wafers are used throughout this series of labs. They are single side polished and contain boron as dopant. From the manufacturer, the thickness, resistivity, and diameter values are given in Tab 2. Prior to the lab, silicon oxide layers were grown on both sides of the silicon wafers via thermal oxidation. In this work, three different structures for three different wafers will be manufactured, the first wafer will be used for the BioMEMS laboratory after the fourth lab session, while the second and third wafer will undergo all six lab sessions.

TABLE II. Silicon Wafer Specifications

Silicon wafer specifications	Values
Diameter	100 mm
Thickness	525±25 µm
Resistivity	1-30 ohm cm

The microfabrication process started with sputtering titanium tungsten (TiW) and gold (Au) on the three wafers. Next, we used photolithography to transfer three different patterns on the wafer using a positive photoresist. The patterned photoresist was used as a mask for the subsequent Au/TiW wet etching and SiO_2 reactive ion etching. Finally, we removed the photoresist and began anisotropic wet etching on the wafer. A complete overview of the series of fabrication processes carried out in six lab sessions can be seen in Fig. 2.

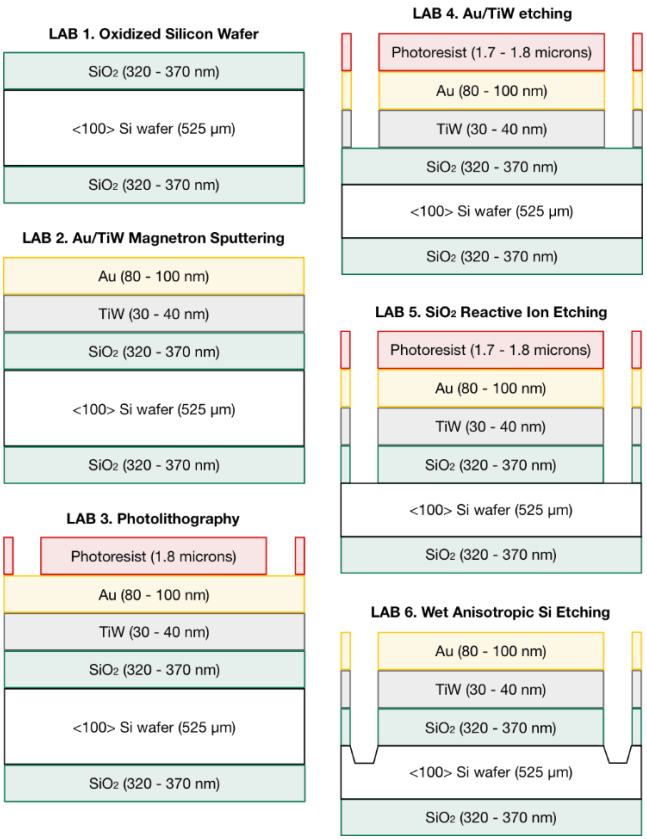


Fig. 2. General overview and outcome of each laboratory session.

In the last two lab sessions, work was undertaken with silicon dioxide reactive ion etching and wet anisotropic silicon etching; only wafer 2 and 3 were subjected to these processes. Although both exhibit square structures, wafer 2 displays smaller square structure while wafer 3 has bigger square structure. Meanwhile, wafer 1 only went through Au/TiW etching and photoresist removal and will be used in the lab sessions for BioMEMS course.

A. Safety and Profilometer (Lab 1)

Laboratory 1 started by introducing general cleanroom safety and good practices. Before the laboratory began it was also important to get acquainted with the safety measures of the diverse chemicals that would be handled throughout the course. It is particularly important to know the properties (effects), preventions measures and first aid responses of each chemical. In total, information about six chemicals was collected. In Tab. 3, the hazardous and prevention statements of these chemicals are listed.

TABLE III. CHEMICAL HAZARDOUS AND PREVENTION STATEMENTS

Chemical name	**Hazardous properties (H-Statements)**	**Prevention (P-Statements)**
Acetone	Highly flammable liquid and vapor. Causes serious eye irritation. May cause drowsiness or dizziness. Repeated exposure may cause skin dryness or cracking.	Keep away from heat, hot surfaces, sparks, open flames, and other ignition sources. No smoking. Ground/bond container and receiving equipment.
Propanol	Highly flammable liquid and vapor. Causes serious eye irritation. May cause drowsiness or dizziness.	Keep away from heat, hot surfaces, sparks, open flames, and other ignition sources. No smoking. Ground/bond container and receiving equipment.
Gold	Harmful if swallowed Harmful in contact with skin Harmful if inhaled Hazardous to the aquatic environment Very toxic to aquatic life	No special precautions required.
Hydrogen Peroxide	Harmful if swallowed. Causes serious eye damage. May cause long lasting harmful effects to aquatic life.	Avoid release to the environment. Wear eye protection.
Potassium Hydroxide	May be corrosive to metals. Harmful if swallowed. Causes severe skin burns and eye damage.	Wear protective gloves/ protective clothing/ eye protection/ face protection.
Positive Photoresist	Highly flammable liquid and vapor. May cause drowsiness or dizziness.	Keep away from heat/sparks/open flames/hot surfaces. No smoking.
		Keep away from breathing in gas/smoke etc. Ground/bond container and receiving equipment.

After the safety measures presentation, the first task was to perform measurements on the ellipsometer and the profilometer. A profilometer is a measurement instrument used to the profile and surface roughness. It can obtain data regarding height, depth, and spacing of peaks and valleys in a surface topography [15]. Profilometers can be of two types: optical or by contact. The profilometer used in this and the other labs was a contact profilometer. This type of profilometer measures the surface finish by setting and moving a thin measurement stylus through the surface section to be analyzed.

We practiced measuring different structures with the profilometer including the thickness of both a positive and negative photoresist structure. Different parameter values like length of sweep and time changed depending on the size of the areas or trenches we desired to measure. Once the measuring process finishes, it was also important to level the results graph by adjusting the reference lines to the highest and lowest points to obtain correct values. This profilometer knowledge proved to be essential for the next lab processes as each time material was deposed or etched from the Si wafer, the wafer was analyzed with the profilometer. In Fig. 3, the profilometer measurement station and a close-up image of the profilometer with a wafer sample in it is exhibited.

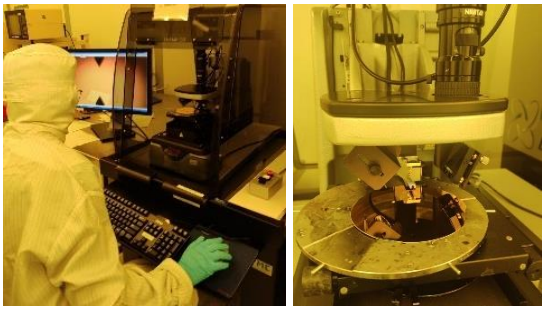


Fig. 3. Measuring with the profilometer (left) and a close-up image of the profilometer (right).

Ellipsometry, on the other hand, measures the relative change in polarization as light is reflected from a material structure [16]. It uses the principle that linearly polarized light changes polarization, becoming elliptically polarized when reflected. This change can be measured and is dependent on the optical properties and thickness of each material. Though it is used in this and other labs primarily to measure layer thickness, it can also provide information about composition, crystallinity, anisotropy, uniformity, etc. [17].

The silicon oxide thickness of each of the three wafers is measured using the ellipsometer. No specific sample preparation is required for measurements using the ellipsometer. The angle of incidence for the measurements was 70 degrees. The sample mode and alignment are both standard.

In this process the wafer is rested on top of the sample area and the measurements are taken just as presented in Fig 4. The results are then shown in the completeEASE software.

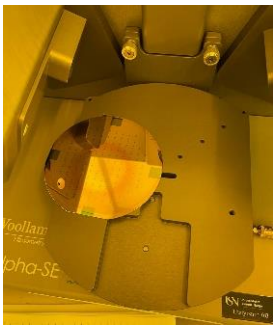


Fig. 4. Measurement with the ellipsometer.

B. *Sputtering (Lab 2)*

Laboratory 2 started with wafer preparation with cleaning, dehydration, and plasma cleaning. We cleaned the wafer to prevent any contamination ruining any subsequent microfabrication processes. Based on the type of contamination (e.g., dust, water vapor, or organic materials), wafer can be dehydrated on a hotplate, cleaned by acetone, isopropyl alcohol (IPA), and deionized water (DI water), and sprayed by pressurized nitrogen gas. A complete thorough cleaning process of the wafer prior to the magnetron sputtering can be seen in Fig. 5.

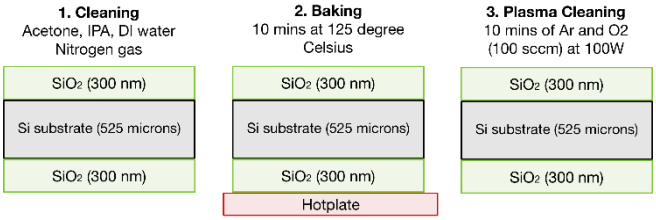


Fig. 5. Wafer cleaning preparation before DC magnetron sputtering process

We used plasma cleaning for each wafer before loading the wafer inside the sputtering machine. We cleaned wafer 2 with a whole set of thorough cleaning, while wafer 1 and 3 was only blown dry by nitrogen gas. Plasma cleaning is done to burn off any leftover organic contaminants from previous cleaning attempts. Parameters presented in Tab. 4 were implemented for each wafer.

TABLE IV. PLASMA CLEANING PARAMETERS BEFORE SPUTTERING

Parameter	Values
Plasma generator power	100 W
O_2 gas flow	100 sccm
Ar gas flow	100 sccm
Time	10 minutes

We used the PVD machine from AJA International to deposit TiW and Au. The machine is capable of DC/RF magnetron sputtering and e-beam evaporation. We used two sputtering targets at the same time, while the machine can have three sputtering target materials and 12 other materials for e-beam evaporation. In this lab, we used magnetron sputtering with TiW (with 90% Ti and 10% W) and Au target. Magnetron sputtering is carried out in a high vacuum environment, opening the chamber may require overnight pumping to reach the proper vacuum level. We used a load lock chamber as a buffer chamber to load the wafer, as shown in Fig. 6.



Fig. 6. Load lock chamber and pressure monitor (left), main chamber and load-lock chamber separator (middle), and wafer holder transfer mechanism (right).

We used the load-lock chamber mechanism to bring a wafer from atmospheric pressure inside the main sputtering chamber. First, we put the wafer on the sample holder and tighten the screw holder, since the wafer will be held upside down. Once the sample holder is inside the load-lock chamber as seen in Fig. 6 (left), we initiated the vacuum pump to bring the chamber to a high vacuum. Once the high vacuum level is reached, the chamber separation is opened, and the mechanism is shown in Fig. 6 (middle) and transferred the sample holder from the load-lock chamber to the main sputtering chamber with the mechanism shown in Fig. 6 (right). Then, the load-lock chamber separation was closed once it was confirmed that the sample holder is in place and the sputtering can begin. A summary of the sputtering process can be seen in Fig. 7.

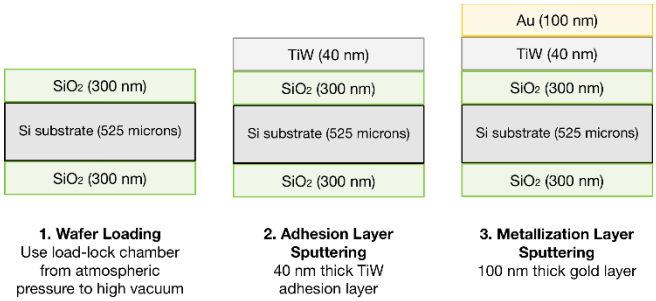


Fig. 7. TiW and Au deposition on Si wafer process

C. *Photolithography (Lab 3)*

We started Laboratory 3 with drying the wafers by blowing nitrogen gas and dehydrating any water vapor on hotplate for 3 minutes at 150 °C. We waited until the wafer cools down to room temperature before loading the wafer inside the Spin 150 machine. We poured a pre-made photoresist solution intended for a single wafer, closed the chamber, and started the pre-programmed spin coating process. Then, the spin coated wafer was taken from the chamber and put on a hotplate where the wafer was soft baked for 1 minute and 30 seconds. The spin coating chamber was cleaned for subsequent use. All wafers were spin-coated with the same recipe and soft-baking conditions shown in Tab. 5.

TABLE V. SPIN COAT AND SOFT BAKE PARAMETERS

Parameter	Values
Maximum rotation speed	1500 rpm
Ramp acceleration	800 rpm/s
Spin coat time	30 s
Soft bake temperature	115°C
Soft bake time	30 s

Then, we used the mask aligner machine to begin the photolithography process. We used a taped plastic mask on a glass for wafers 1 and 3, and a glass mask for wafer 2 with small square structures. The glass mask is loaded inside a metal enclosure and installed on the aligner machine as can be seen in Fig. 8 (left). This machine ensured a soft contact between the mask and the wafer during the UV exposure.

In this lab, only one mask is used for each wafer therefore no complex alignment is required. We only aligned the mask to ensure no space was wasted on the wafer. We used the two joysticks to align the mask and the wafer as shown in Fig. 8 (right). UV exposure can be started once the mask and the wafer have been properly aligned. The photoresist was exposed with 274 watts of UV power for 70 seconds.



Fig. 8. BioMEMS mask loaded on the aligner (left) and the alignment process by moving the joystick (right)

Exposed photoresist was developed by the MF-319 developer. The profilometer was used to evaluate photoresist thickness and uniformity with measurements taken at multiple points. Then, the wafer was placed on a hotplate and started hard baking at 115 °C for 3 minutes and it was allowed to rest until the wafer was approaching room temperature. Then, the thickness was measured again with a profilometer to study the effect of hard baking photoresist. The same series of photolithography process were carried out for all wafers, as summarized in Fig. 9.

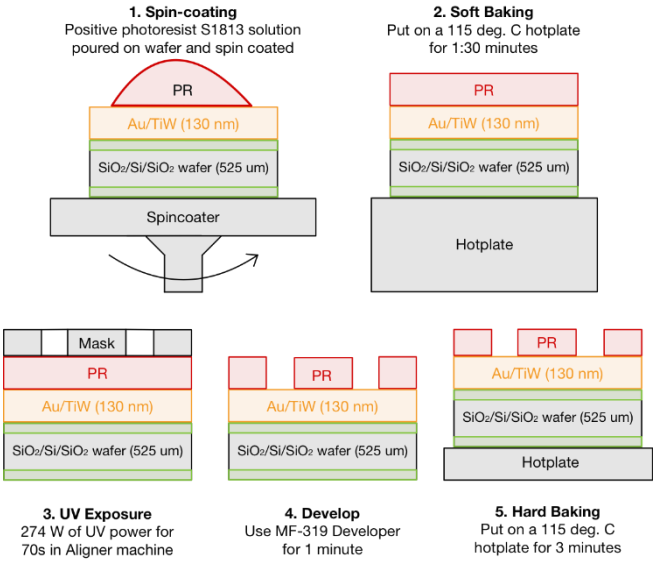


Fig. 9. Summary of the photolithography laboratory process

D. Au/TiW etching (Lab 4)

Once each of the three wafers were covered with the positive photoresist and photolithography was performed to remove the photoresist from necessary areas, the layer thickness measurement was performed again using profilometer for each of the wafers. Measurement was done between areas having the photoresist to zones devoid of photoresist which would give the thickness of the photoresist layer alone. This would later aid in calculating thickness of the gold and tungsten-titanium layers on the wafer, and in turn, help verify all the measurements against the estimated thickness from sputtering and spin coating methods. For the study, measurement was performed only at two positions on the wafer due to time constraints but ideally multiple measurements at different locations is suggested. The position of measurement was roughly noted to repeat the measurement at the same location in further stages.

The next step was to etch away the gold layer from each of the wafers. This was performed using the most common etchant iodine-iodide solution for patterning gold, which has an etching rate of 0.5 to 1 microns per minute at room temperature [18]. The etchant was created using mixture of potassium iodide (KI), iodine (I_2) and water. Each of the wafers were immersed in the etchant for a duration of 40 seconds, later washed in DI water and dried using nitrogen gas. The anodic reaction and cathodic reaction in the etching process are given as [18]:

$$Au + 2I^- \rightarrow AuI_2^- + e^-$$
$$I_3^- + 2e^- \rightarrow 3I^-$$

The photoresist mask protects the Au layer beneath it from being etched away though some undercut may happen due to isotropic wet etching, and the etchant reacts mostly with the exposed gold layers removing them completely. Thus, in areas where the photoresist was absent, the TiW layer is visible after the gold etching step. Layer thickness measurement was again performed using profilometer this time obtaining the thickness from the TiW layer to top of photoresist, which is the sum of layer thickness of Au and the photoresist layers. The thickness of the gold layer can be calculated from here by subtracting the previously calculated thickness of photoresist. The measurement again was performed at the previous two positions on the wafer.

TiW layer etching was then performed on each of the wafers using a mixture of 30% concentration hydrogen peroxide (H_2O_2) with ethanol maintained at a temperature of 50°C. The wafers were immersed in the solution for 3 minutes, later washed with DI water and dried by blowing nitrogen gas. The silicon dioxide layer was thus visible after the TiW layer was removed. Profilometer measurements were then taken at the known positions, this time going from the top of photoresist layer till the top of silicon dioxide layer. By this means, the TiW layer thickness was obtained from the combined thickness of Au, TiW and photoresist layers.

In order to ensure that the etching process was successful throughout the wafer and no large metal residues were present, continuity test was done using a multi meter over the etched area as shown in Fig. 10.

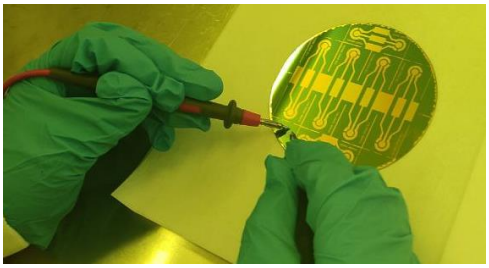


Fig. 10. Continuity test using multimeter on Au/TiW etched wafer

Wafer 1 exhibited a biosensor pattern printed on it. The fabrication steps for wafer 1 was complete and silicon etching was not to be performed on it. Thus, photoresist removal was carried out on this wafer alone using acetone, washed with isopropyl alcohol, DI water and dried using nitrogen gas. Plasma cleaning using oxygen was next performed to remove any photoresist residues. We performed a profilometer measurement on wafer 1 before and after plasma cleaning to study the impact of plasma cleaning. These parameters were used for plasma cleaning: plasma power of 300 watts, oxygen gas flow at 300 cubic centimeters at STP (sccm), and a duration of 5 minutes.

E. SiO_2 Reactive Ion Etching (Lab 5)

Reactive ion etching (RIE) is used to dry etch the silicon oxide from the wafers. The RIE machine that was used in the lab was the PlasmaPro 100 Estrelas RIE platform. The SiO_2 reactive ion etching was only performed on wafers 2 and 3. Wafer 1 did not go through the SiO_2 reactive ion etching or the subsequent wet silicon etching.

First, we placed the wafer in the load-lock chamber and then pumped out the air in the chamber. The load-lock chamber can be observed in Fig. 11 When there is vacuum inside the chamber the wafer is transported to the main chamber. Once the wafer is inside the main chamber, the gas starts flowing. The next step is to start the HF and inductive coupling plasma (ICP) power and begin the etching process. The etching process time was set to 3 minutes. The pre-programmed gas recipe was used as shown in Tab. 6 for the RIE process.



Fig. 11. PlasmaPro 100 Estrelas load-lock chamber.

After the etching process is finished, the wafer is transported from the main chamber to the load-lock chamber, where air and pressure is restored. Once the pressure inside the chamber reaches atmospheric pressure values it can be open, and the wafer is extracted. This process was repeated for both wafers.

TABLE VI. GAS RECIPE FOR THE SIO2 RIE PROCESS

Parameter	Values
APC/LPS	10 mTorr
CHF_3 gas flow	17 sccm
Ar gas flow	33 sccm
ICP power	1500 W
HF power	50 W
Time	3 minutes

After the processes were finished for both wafers, we measured the thickness of SiO_2 on the newly etched layers with the ellipsometer. For these measurements, it was necessary to check that the incidence point of the polarized light hit the etched feature. Due to the reflectivity of the wafer, the incoming light was difficult to spot. We used a small piece of paper on top of the wafer to spot the incoming light. We were able to align the wafer properly so we could measure SiO_2 thickness on the etched feature. This method to correctly place the wafer can be seen in Fig. 12, where the incoming light hitting the paper is circled in red. Measurements were taken of the etched areas for both wafers. This time the angle of incidence for the measurements was 65 degrees. The results are then shown in the completeEASE software.

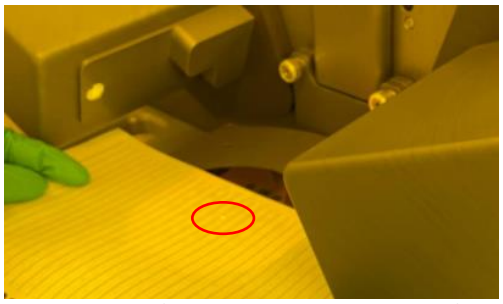


Fig. 12. Detection of the incoming light with a piece of paper.

F. Silicon Anisotropic Wet Etching (Lab 6)

In preparation for the wet etching of the silicon layer, the photoresist residue on each wafer was eliminated by using a combination of three cleaning processes. Initially, each wafer was cleaned twice with acetone, IPA, and DI water in the specified sequence and dried using papers. Next, the combined depths of the etched cavities were measured at two positions on each wafer using profilometer. Each wafer was then immersed in acetone and put in an ultrasonic bath (shown in Fig. 13) for 8 minutes and 5 minutes respectively for wafer 2 and 3. Then the wafers were rinsed with IPA and DI water, and dried with nitrogen gas; cavity depth measurements were also performed.



Fig. 13. Ultrasound bath used in the photoresist removal process.

In addition, plasma cleaning was performed on each wafer using oxygen gas with a gas flow rate of 400 cubic centimeters at STP, a power supply of 400 watts, and a chamber pressure of 130 Pascal for 3-4 minutes for both the wafers.

Following this, measurements of the cavity depths in each location were measured, just as they had been in the preceding washing procedures. We etched the exposed silicon layer by immersing the wafer in a 10% potassium hydroxide (KOH)

solution at 75 °C for 30 minutes, while the bath was regularly stirred. Fig. 14 shows the wafer being immersed in the KOH solution. We maintained safety measures by wearing goggles and safety helmet throughout the wet etching process. Parameters for photoresist removal and cleaning are tabulated in Tab. 7.

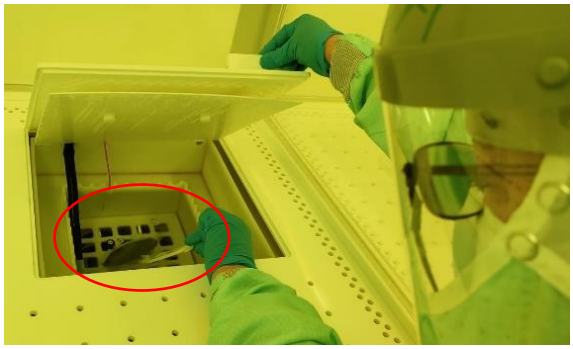


Fig. 14: Wafer immersed in 10% KOH solution for anisotropic Si etching.

TABLE VII. PHOTORESIST REMOVAL & CLEANING PARAMETERS BEFORE SI WET ETCHING

Wafer 2	**Ultrasound Bath**	**Plasma Cleaning**		
	Time: 8 min	Power: 400 W	O_2 Gas Pressure: 400 sccm	Time: 3 min
Wafer 3	**Ultrasound Bath**	**Plasma Cleaning**		
	Time: 5 min	Power: 500 W	O_2 Gas Pressure: 400 sccm	Time: 4:30 min

As the etching was done, we measured thickness on various positions of the wafers. Further analysis of measurements results and discussions are presented in the Results and Discussions section.

III. RESULTS AND DISCUSSIONS

During each laboratory, measurements were taken to check the process quality through the profilometer and ellipsometer; these profilometer graphs and ellipsometer readings were applied to exhibit the thin film deposition and etching results. The artefacts will be highlighted prior to, and after cleaning the wafer; moreover, discussion on the possible reasons of such findings will be assessed.

A. Safety and Profilometer

Fig. 15 presents a measurement of a negative photoresist structure. The green and red bars indicate the reference lines, one should be placed on the lowest point and the other on the highest. This image has already been leveled as evidenced by the straight lines. It can be clearly seen how the profilometer measures a valley in the structure that is 93.4 microns deep.

Data obtained by the ellipsometer includes spectroscopic ellipsometry (SE) data, angle offset, and total thickness. The angle of incidence used was 70 degrees. In Fig. 16, it is possible to observe the completeEASE software screen where the ellipsometer results data is shown. These results were obtained for wafer 3.

In Tab. 8, the measured silicon oxide thickness is displayed alongside the angle of incidence used on each wafer. Several decimals shown in Fig. 16 were omitted for significant figure consistency.

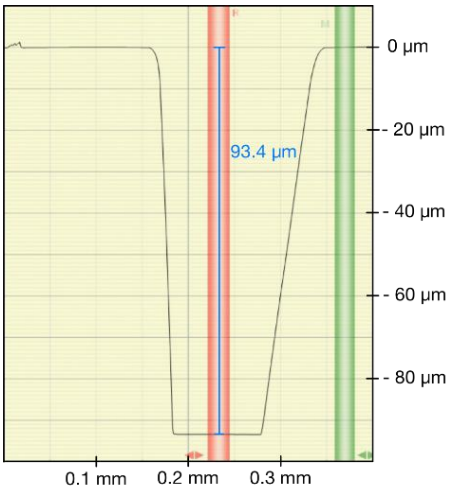


Fig. 15. Profilometer read of negative photoresist on Si wafer.

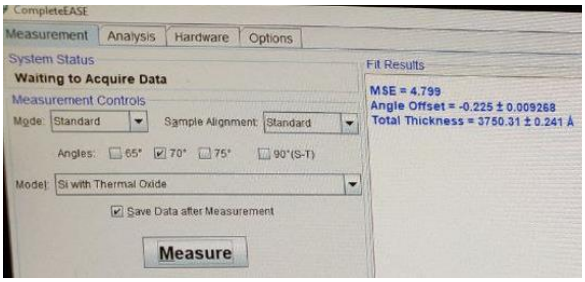


Fig. 16. Ellipsometer result shown on completeEASE window.

TABLE VIII. SILICON OXIDE THICKNESS FOR EACH WAFER

Wafer No.	Silicon Oxide Thickness (Å)	Angle of incidence
1	3774.6 ± 0.2	70°
2	3312.6 ± 0.2	70°
3	3750.3 ± 0.2	70°

Taking the results from the ellipsometer measurement, it is possible to know that for both wafer 1 and 3 a similar layer of thickness of around 370 nanometers was formed, while wafer 2 received a significantly less thick silicon oxide layer of around 330 nanometers. The measurements from the ellipsometer show a very high precision min/max range, down to decimals of angstroms, computed by the completeEASE software.

Because of the transparent nature of silicon oxide at certain wavelengths, measurements with an ellipsometer are not limited by the thickness of the material. This indicates that the thickness measurements of silicon oxide are very practical as ellipsometer measurements are contactless, non-destructive, and the sample does not require special preparations.

B. Sputtering

PVD controller gave an estimation of thickness from the sputtering chamber parameters set in the machine and the deposition rate sensor inside the chamber. Parameters used in the deposition rate estimation are the DC power, pressure, Ar gas flow, and target material. From the deposition rate and time, the software was able to provide us a thickness estimate for both TiW and Au, summarized in Tab. 9 and Tab. 10.

TABLE IX. SPUTTERING PARAMETERS FOR TIW LAYER

Parameter	Parameter Values		
	Wafer 1	Wafer 2	Wafer 3
DC Power	40 W	40 W	40 W
Gas flow rate	10 sccm	10 sccm	10 sccm
Deposition rate	0.22 Å/s	0.22 Å/s	0.22 Å/s
Throttled pressure in main chamber	7.40 mTorr	7.49 mTorr	7.46 mTorr
Thickness	35 nm	30 nm	40 nm

TABLE X. SPUTTERING PARAMETERS FOR AU LAYER

Parameter	Parameter Values		
	Wafer 1	Wafer 2	Wafer 3
DC Power	25 W	25 W	30 W
Gas flow rate	12 sccm	12 sccm	12 sccm
Deposition rate	0.35 Å/s	0.35 Å/s	0.42 Å/s
Throttled pressure in main chamber	8.88 mTorr	8.89 mTorr	8.83 mTorr
Thickness	80 nm	100 nm	100 nm

TiW is used as an adhesion layer and only 30-40 nanometers thin layer is needed; different thicknesses were observed from different deposition time. As seen in Tab. 10, increasing the DC power will also increase the deposition rate of gold. Thickness of Au was estimated to be 100 nanometers for Wafer 2 and 3 since the sputtering is stopped once 100 nanometers thick layer is reached. However, for the second wafer, we did not switch the target material (from TiW to Au) on the controller software. Therefore, deposition rate estimation by the software was not accurate. Although 100 nm thickness of Au was estimated, the deposited Au could be more than anticipated.

Once the sputtering deposition is complete, we opened the main chamber and unload the wafer holder to the load-lock chamber. Air was pumped in from the atmosphere so the wafer can be extracted. The wafer exhibited a highly reflective gold layer successfully sputtered all over the wafer except for the part covered by the wafer holder at the edges. We performed a tape adhesion test, and the gold thin film did not come off, showing a good adhesion. The wafer was stored inside a holder for the next lab session as shown in Fig. 17.

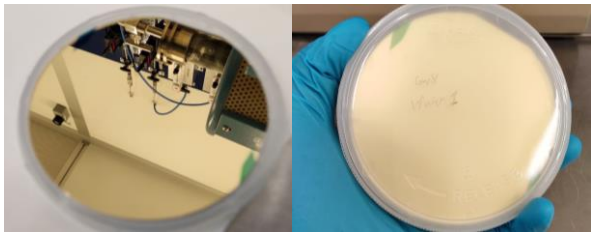


Fig. 17. Wafer 1 after Au/TiW sputtering and adhesion tape test

C. Photolithography

We measured different points in each wafer to study photoresist thickness and its uniformity. However, due to limited allotted time, we could only take two samples in each wafer. Measurements are done directly after developing the photoresist and after hard baking process to see the impact of hard baking to photoresist thickness. A slight shrinkage of photoresist can be noticed after the hard baking process. For example, on wafer 2, before hard baking the photoresist was 1.9 microns and shrunk to 1.85 microns afterwards. All measurements of this effect can be seen in Tab. 12.

TABLE XI. PHOTORESIST THICKNESS MEASURED AFTER SOFT BAKE AND HARD BAKE

Wafer No.	Thickness after Soft Bake (nm)		Thickness after Hard Bake (nm)
	Point 1	Point 2	
1	1839	1845	1792
2	1974	1901	1846
3	1777	1714	1705

Aside from the observed photoresist shrinkage after hard baking, a “bat ear” artefact was also noticed in the profilometer measurement. Probably, this originated from hardened photoresist residue at the edge of the structure, this artefact has a linewidth of 10 microns and a height of less than 100 nm. An example of this artefact can be observed in our photoresist thickness measurement done on Wafer 2, shown in Fig. 18.

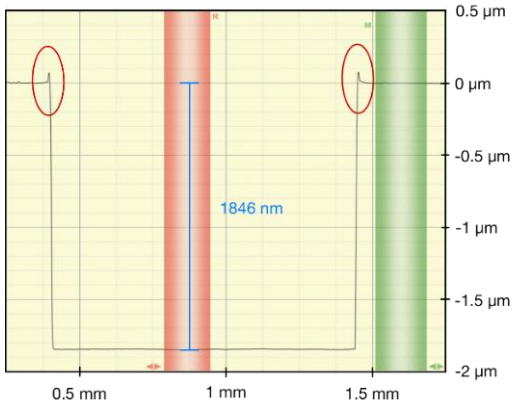


Fig. 18. Photoresist thickness measurement on Wafer 2 after hard baking process showing a "bat ear" artefact marked in red.

D. Au/TiW etching (Lab 4)

Layer thickness measurements taken using profilometer on each of the wafers are documented below. Height measurements were made at two positions on the wafers after each of the photolithography, Au etching, TiW etching and photoresist removal stages. Estimated layer thickness for gold layer after PVD was 80 nanometers for the first wafer and 100 nanometers for the second and third wafers.

The calculated layer thickness of gold for wafer 1 matches the estimate for position one but varies for position two. There is considerable variation also for wafer 2 but less deviation for wafer 3 again indicating that the estimate may not always have high accuracy. For the multimeter continuity test, no audio output signal was observed even after probing at multiple etched locations indicating that TiW and Au was etched away.

TABLE XII. PHOTORESIST, GOLD, TITANIUM TUNGSTEN LAYER MEASURED THICKNESS

Wafer No.	PR Thickness (µm)		PR + Au Thickness (µm)		PR + Au + TiW Thickness (µm)	
	Pos. 1	Pos. 2	Pos. 1	Pos. 2	Pos. 1	Pos. 2
1	1.8	1.75	1.88	1.86	1.96	1.91
2	1.82	1.89	1.98	2.06	2.06	2.09
3	1.73	1.66	1.82	1.79	1.90	1.86

TABLE XIII. CALCULATED GOLD LAYER THICKNESS

Wafer No.	Gold Thickness (nm)	
	Pos. 1	Pos. 2
1	80	110
2	160	170
3	90	130

For wafer one, profilometer measurement taken after photoresist removal is shown in Fig. 19 and another—taken after plasma cleaning step—is given in Fig. 20. A much smoother surface profile was expected after the plasma cleaning stage but the measurements showed some non-uniformity on surface as seen from the height variations in Fig. 20.

This may be due to the oxidized residues or other contaminants. Profilometer plots would not help in identifying the reason for this variation and further investigation using surface measurement techniques such as optical microscope or interferometry may be required.

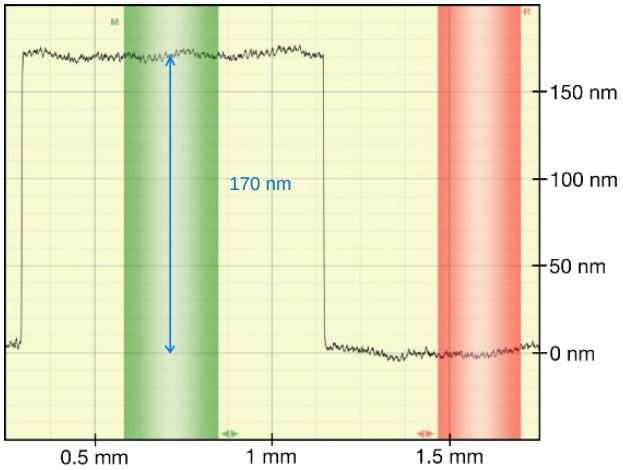


Fig. 19. Combined thickness of Au and TiW layers on Wafer 1

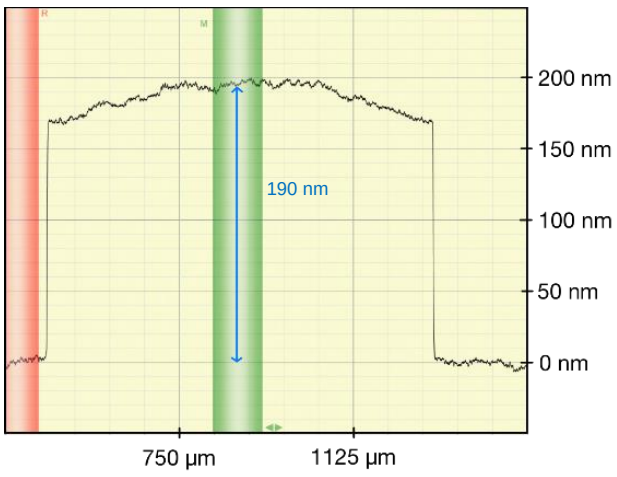


Fig. 20. Combined thickness of thickness of Au and TiW layers on Wafer 1 after plasma cleaning

The sum of thickness of Au and TiW layers measured at position 2 of Wafer 1 as shown in Fig. 19 gave a reading of 170 nanometers. After plasma cleaning the thickness measurement at the same position resulted in 190 nanometers. This increase in thickness can be attributed to the removal of photoresist residues at that position after plasma cleaning.

E. Silicon Dioxide Reactive Ion Etching

Data obtained by the ellipsometer includes spectroscopic ellipsometry (SE) data, angle offset, and total thickness. The angle of incidence used was 65 degrees. In Tab. 14, it is possible to observe the silicon oxide thickness and used angle of incidence for each of the wafers.

TABLE XIV. SILICON THICKNESS FOR EACH WAFER

Wafer No.	Silicon Oxide Thickness (Å)	Angle of incidence
2	26.1 ± 0.5	65°
3	28.3 ± 0.6	65°

It is possible to observe from the results in Tab. 14 the effects of the silicon oxide etching process. By comparing the information from Tab. 8 and Tab. 14, for wafer 2 the silicon oxide layer thickness has reduced from 331.2 nanometers to just 2.6 nanometers, and the layer thickness for wafer 3 dropped from 370 nanometers to 2.8 nanometers. More than 300 nanometers of silicon oxide were etched with 3 minutes of RIE process, indicating a 100 nanometer per minute etching rate. These results show the efficiency of the RIE technique and why it is one of the most used SiO_2 etching methods today.

F. Silicon Anisotropic Wet Etching

Each wafer is cleaned using several techniques before continuing to wet etching of silicon, and the results of each cleaning stage are presented in Tab. 15. From the data even after RIE, some of the residual photoresist exists on the wafer. For wafer 2, plasma cleaning was done after the ultrasound bath and wafer cleaning process mentioned in Silicon Anisotropic Wet Etching (Lab 6) section. The result for wafer 2 is not consistent with position 1 and 2. Same goes for wafer 3 although, in this case, the plasma cleaning was done before the ultrasound bath and washing. The difference in the result may be due to the residual photoresist left behind in that position of measurement of the wafer. Also, there may be some excess material from ultrasound bath. Another reason may be due to the difference in the position of the measurements.

TABLE XV. COMBINED AU, TIW, AND SiO_2 THICKNESS FOR EACH WAFER

Photoresist Residue Removal (Wafer 2)	Thickness of Position 1 (nm)	Thickness of Position 2 (nm)
Washing + Ultrasound	626	613
Washing + Ultrasound Bath + Plasma Cleaning	634	617
Photoresist Residue Removal (Wafer 3)	**Thickness of Position 1 (nm)**	**Thickness of Position 2 (nm)**
Washing + Plasma Cleaning	656	643
Washing + Plasma Cleaning + Ultrasound Bath	655	637

The data listed in Tab. 16 show the thickness of the combined layer after the anisotropic wet etching of silicon. The etched part of silicon can be found by subtracting the values displayed in Tab. 16 & Tab. 17. From the thickness of

the etched silicon, the etched rate can be compared with a reference value described in the next paragraph.

TABLE XVI. COMBINED AU, TIW, SiO_2, AND SI THICKNESS FOR EACH WAFER

Wafer No.	Thickness (nm)	
	Pos. 1	Pos. 2
2	32311	32359
3	30997	31027

Tab. 17 shows the thickness values of etched silicon after anisotropic etching. If the rate of Si <100> etching at 76°C in 10% solution of KOH is 65 microns per hour [19], the etching depth for 30 minutes can be calculated as 32.5µm. We observed similar Si etching depth (with only a difference of ~6.64%) to the theoretical values found in the reference paper with similar etching parameters. This indicated that the silicon etching was correctly preformed. However, we also note that when compared to RIE, the wet Si etching rate is slower.

TABLE XVII. CALCULATED SILICON ETCH DEPTH FOR EACH WAFER

Wafer No.	Etch Depth (nm)	
	Pos. 1	Pos. 2
2	31677	31741
3	30342	30390

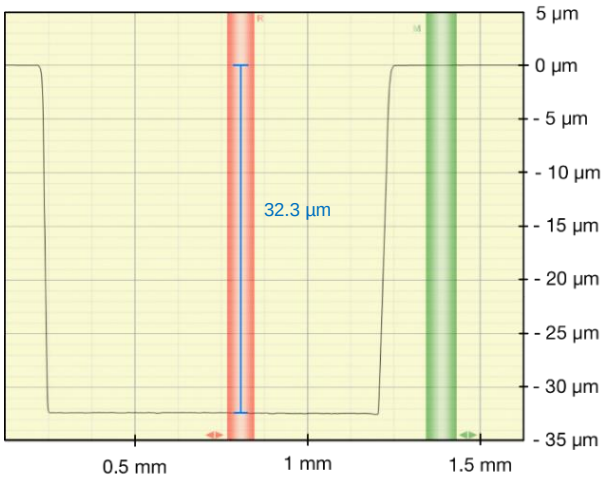


Fig. 21. Combined thickness of Au, TiW, SiO_2, and Si layers of Wafer 2 after silicon anisotropic etching.

Fig. 21 depicts the thickness of Au, TiW, SiO_2, and Si layers after silicon etching for wafer 2. From the image, it can be observed that, when compared to the previous edges of the surface of the wafer, after all the cleaning procedures the surface of the wafer is smoother and more consistent. We can also observe the anisotropic behavior of the <111> sidewalls in Fig. 21. This anisotropic behavior is also visible in the final wafers after Au, TiW, SiO_2, and Si etching shown in Fig. 22.

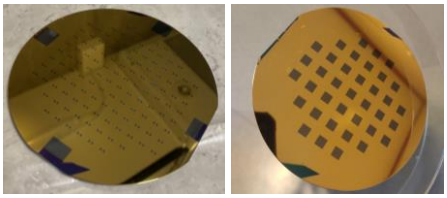


Fig. 22 Wafer 2 (left) and wafer 3 (right) after Au, TiW, SiO_2, and Si etching

All the fabrication processes were successfully accomplished for the three wafers and satisfactory results were achieved. Process parameters and estimation from the measurements were confirmed effectively. However, some anomalies are observed after cleaning process. It probably may be related to the plasma cleaning parameters having unintended results, however from linewidth scan measurements we carried out on the profilometer, it is not possible to establish the veracity of that statement. In retrospect, the use of optical microscopy and interferometry technique would have been of significant support to obtain clearer 2D images of each sample where these inconsistencies were noted.

IV. CONCLUSIONS

Sputtered Au/TiW layer exhibited high reflectivity indicating uniform distribution, However, the thickness estimation derived from the controller were not accurate. Subsequent photolithography process measured show a quite uniform distribution of photoresist, although artefact of photoresists residue is observed near the edges. Thickness of the photoresist were sufficient for next etching processes.

Etching of Au and TiW was carried out using chemical etchants where the solution concentration, time of exposure of wafer to etchant and the parameters like temperature had to be precisely controlled. The entire process was carried out manually, but the layer thickness results were comparable to the those from the PVD process though some surface non-uniformity was observed after plasma cleaning.

The silicon oxide RIE process proved to be a quick and efficient way of etching the silicon oxide layer. Being an automated process meant that the same amount of material was etched resulting in silicon oxide thickness values that were in proximity. It is important to note that another layer of SiO_2 was formed after the RIE process. However, this additional oxide layer did not affect the next etching process steps.

Anisotropic wet etching, although a slow process compared to RIE, it showed similar results when compared to the existing etched rate data. It can be inferred that anisotropic wet etching was done correctly. Nevertheless, it is worth mentioning that the results were dependent on the process the wafers were cleaned and the or der they were cleaned. Further improvement could be done by keeping these dependent parameters the same for each measurement.

In conclusion, although there are some quirks and anomalies observed in individual processes, it was demonstrated that the results were satisfactory, meeting the initial expectations. More measurements techniques can be used to pinpoint the reasons of encountered anomalies, but this would be trivial on a simple structure fabricated on experimental wafer.

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