PERSONAL DETAILS

Name: **Shady Agwa**

Formal Name: **Shady Onsey Haleem Rizkalla**

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I earned my PhD in Electronics Engineering, with a special focus on VLSI Design, from the **American University in Cairo** (Egypt, 2018). My PhD developed resilient, Low-Power ASICs that mitigate runtime Process, Voltage, and Temperature (PVT) variations, without sacrificing the overall performance. In alignment with my PhD research, I had **2 tape-outs (Chips)** and published **5 papers**, as first author, in highly ranked transactions and conferences like **IEEE TCAS-I, TCAS-II**, and **ISCAS**. Then, I joined **Cornell University** (USA, 2019-2020) for two years as a **Postdoctoral Associate**, where I worked under the supervision of **Prof. Christopher Batten** and gained hands-on expertise in Large-Scale Digital Hardware Architectures for ML using advanced technology nodes (TSMC28nm, GF12nm). I also collaborated with teams from **Princeton University** and **University of Washington**. My contribution at Cornell University led to **a tape-out** and **7 publications**, including flagship venues like **HPCA, IEEE Solid-State Circuits Letters, CICC,** and **ISCAS**. In 2021, I joined the **Centre for Electronics Frontiers (CEF)** as a Research Fellow at the **University of Edinburgh** (previously at the **University of Southampton**) (UK) to work with **Prof. Themis Prodromakis**, a world-leading expert in emerging devices (RRAMs). I also collaborated with **Imperial College London** (UK) to build MELITA (a characterization chip of a million RRAM devices) and I established **3 new projects** on Energy-Efficient AI Hardware. At CEF, I had **22 publications** in prestigious venues, including **5 IEEE TCAS-I, 1 IEEE TCAS-AI, 1 IEEE TKDE, 1 IEEE JxCDC, 1 IEEE OJCAS, 5 ISCAS, and 2 NEWCAS**. I also filed **6 patents** on energy-efficient AI Hardware. I have also contributed significantly to **8 Chips**, and I was a **Researcher Co-I of "Prosensing"**, a UKRI grant of £1.45M. In August 2026, I joined the Department of Electrical & Electronic Engineering, the **University of Manchester** (UK) as a Lecturer in Electronic Systems.

QUALIFICATIONS

23-6-2018 **PhD in Electronics Engineering,**
Department of Electronics and Communications Engineering, The American University in Cairo, Egypt. Supervisor: Prof. Yehea Ismail

2011 **MSc in Electrical Engineering,**
Electrical Engineering Department, Assiut University, Egypt.

2006 **BSc in Electrical Engineering,**
Electrical Engineering Department, Assiut University, Egypt.

CURRENT POSITION

2026 - Present **Lecturer in Electronic Systems,**
Department of Electrical & Electronic Engineering, The University of Manchester, UK.
Member of Sensors & Electronics (SAE) Group, and the International Centre for Neuromorphic Systems (ICNS).

PREVIOUS POSITIONS

2022 - 2026 **Research Fellow** in AI-Specific Integrated Circuits and Systems.
Centre for Electronic Frontiers, School of Engineering, The University of Edinburgh, UK.

2021 - 2022 **Senior Research Fellow** in AI Hardware
Centre for Electronic Frontiers, University of Southampton, UK.

2019 - 2021 **Postdoctoral Associate** in Computer Architecture and Digital VLSI
Computer Systems Lab, Cornell University, USA.

2018 **Postdoctoral Researcher** in Digital VLSI
Center of Nanoelectronics & Devices, The American University in Cairo, Egypt.

2012 - 2018 **Research & Teaching Assistant**
Center of Nanoelectronics & Devices, Zewail City of Science & Technology, Egypt.

PATENTS

2026 **"Exponential Bitstream Based Computing System and Method"**
Inventors: **Shady Agwa**, Yihan Pan and Themis Prodromakis.
PCT App. No. PCT/GB2613272

2025 **"A Computer Architecture for Matrix-Matrix Multiplication"**
Inventors: **Shady Agwa**, Ahmed J. Abdelmaksoud and Themis Prodromakis.
PCT App. No. PCT/GB2025/051975

2025 **"A Computer Architecture for a Convolutional Neural Network"**
Inventors: Cristian Sestito, **Shady Agwa** and Themis Prodromakis.
PCT App. No. PCT/GB2025/051346

2025 **"Memory Cell Device"**
Inventors: **Shady Agwa**, Georgios Papandroulidakis and Themis Prodromakis.
PCT App. No. PCT/GB2025/051942

2024 **"A Memory Computing Device, a Method of Operating the Same and an AI System Including the Same"**
Inventors: **Shady Agwa** and Themis Prodromakis.
PCT App. No. PCT/GB2024/05052

2023 **"A Memory Device"**
Inventors: Alex Serb, Yihan Pan, **Shady Agwa**, Mohammed Mughal, Adrian Wheeldon, Sachin Maheshwar, and Themis Prodromakis.
PCT App. No. PCT/GB2023/05324

GRANTS

January 2024 **ProSensing: Low-Power, High-Speed, Adaptable Processing-In-Sensing Capability"**
UKRI EPSRC National Security Sandpit 2, Budget: £1,457,851.00, 3 Years.
Prof. Themis Prodromakis (PI) & Dr. **Shady Agwa (Researcher Co-I)**, University of Edinburgh (UK). Prof. Eiman Kanjo (Co-I), Nottingham Trent University (UK). Prof. Antonio Hurtado (Co-I), University of Strathclyde (UK).

INVITED TALKS

March 2026 "A New Generation of AI-Specific Integrated Circuits & Systems AISICS"
Invited Talk at **Imperial College London, UK.** (In Person)

February 2026 "A Next Generation of AI-Specific Integrated Circuits & Systems AISICS"
Invited Talk at **The University of Tennessee, Knoxville, USA.** (Online)

November 2025 "AI-Specific Circuits and Systems Towards A New Hardware-Driven AI Computing Paradigm"
Invited Talk at Batten Research Group, **Cornell University, USA.** (In Person)

October 2025 "IMBC: RRAM-based In-Memory Bitstream Computing for A Next Generation of AI Hardware"
Talk at the 8th International Conference on Memristive Materials, Devices & Systems, **MEMRISYS, UK**. (In Person)

September 2024 "Digital In-Memory Stochastic Computing Architectures"
Invited Talk at **CAS-sponsored Seasonal School** on " Neuromorphic Computing and Logic In Memory Computing Using Non-Volatile Memory Devices", **India.** (Online)

October 2023 "Bridging The Gap Between Emerging Technologies And AI Hardware"
Invited Talk at 8th European Congress on Advanced Nanotechnology and Nanomaterials, **London, UK**. (In Person)

MEMBERSHIP

IEEE Senior Member & IEEE CAS Member.
Associate Editor at IEEE Open Journal of Circuits and Systems.

PAPER RECOGNITION

2026 DiP Paper, DOI: 10.1109/TCSI.2025.3591960,
The Highlight of IEEE Transactions on Circuits & Systems I, TCAS-I, 2026 January Issue.
IEEE TCAS-I is the flagship Transaction of the IEEE CAS Society.

CO-ADVISING

Postdoctoral Associates	1- Dr. Georgios Papandroulidakis, Analog Content-Addressable Memory for Edge Classification (ProSensing). 2- Dr. Cristian Sestito, Convolution Neural Networks CNNs Acceleration using Systolic Arrays (TrIM). 3- Dr. Yihan Pan, Digital In-memory Computing Architectures for Matrix Multiplication Acceleration (OISMA).
PhD Students	1- Ahmed Abdelmaksoud, AI Hardware Acceleration for Large Language Models (LLMs) using Systolic Arrays (DiP). 2- Bochen Ye, Large-Scale Digital AI Systems for Large Language Models (LLMs) (BenDi). 3- Eleni Tselepi, Large-Scale Digital AI Systems for Convolution Neural Networks CNNs Acceleration.

SELECTED PAPERS

For the full list, please visit https://scholar.google.com/citations?user=cSfD758AAAAJ

1. Mifsud et al., "A Multi-Bit CMOS Characterization Platform for One-Million Resistive Switching Devices," in **IEEE Transactions on Circuits and Systems I**: Regular Papers, vol. 73, no. 9, pp. 5918-5931, Sept. 2026, doi: 10.1109/TCSI.2026.3680429.
2. S. Agwa, Y. Pan, G. Papandroulidakis and T. Prodromakis, "OISMA: On-the-Fly In-Memory Stochastic Multiplication Architecture for Approximate Matrix Multiplication," in **IEEE Journal on Exploratory Solid-State Computational Devices and Circuits**, vol. 12, pp. 56-64, 2026, doi: 10.1109/JXCDC.2026.3680281.
3. K. Woodward, E. Kanjo, G. Papandroulidakis, S. Agwa and T. Prodromakis, "A Hybrid Edge Classifier: Combining TinyML-Optimised CNN With RRAM-CMOS ACAM for Energy-Efficient Inference," in **IEEE Transactions on Knowledge and Data Engineering**, vol. 38, no. 4, pp. 2122-2135, April 2026, doi: 10.1109/TKDE.2026.3655717.
4. C. Sestito, S. Agwa and T. Prodromakis, "TrIM, Triangular Input Movement Systolic Array for Convolutional Neural Networks: Dataflow and Analytical Modelling," in **IEEE Transactions on Circuits and Systems for Artificial Intelligence**, vol. 2, no. 3, pp. 197-210, Sept. 2025, doi: 10.1109/TCASAI.2025.3591073.
5. A. J. Abdelmaksoud, S. Agwa and T. Prodromakis, "DiP: A Scalable, Energy-Efficient Systolic Array for Matrix Multiplication Acceleration," in **IEEE Transactions on Circuits and Systems I**: Regular Papers, vol. 73, no. 1, pp. 283-293, Jan. 2026, doi: 10.1109/TCSI.2025.3591960.
6. G. Papandroulidakis, S. Agwa, A. Cirakoglu and T. Prodromakis, "A 9T4R RRAM-Based ACAM for Analogue Template Matching at the Edge," in **IEEE Transactions on Circuits and Systems I**: Regular Papers, vol. 72, no. 10, pp. 5545-5558, Oct. 2025, doi: 10.1109/TCSI.2025.3545257.
7. C. Sestito, S. Agwa and T. Prodromakis, "TrIM, Triangular Input Movement Systolic Array for Convolutional Neural Networks: Architecture and Hardware Implementation," in **IEEE Transactions on Circuits and Systems I**: Regular Papers, vol. 72, no. 5, pp. 2263-2273, May 2025, doi: 10.1109/TCSI.2024.3522351.
8. A. Li et al., "CIFER: A Cache-Coherent 12-nm 16-mm2 SoC With Four 64-Bit RISC-V Application Cores, 18 32-Bit RISC-V Compute Cores, and a 1541 LUT6/mm2 Synthesizable eFPGA," in IEEE Solid-State Circuits Letters, vol. 6, pp. 229-232, 2023, doi: 10.1109/LSSC.2023.3303111.
9. K. Al-Hawaj et al., "EVE: Ephemeral Vector Engines," 2023 **IEEE International Symposium on High-Performance Computer Architecture (HPCA)**, Montreal, QC, Canada, 2023, pp. 691-704, doi: 10.1109/HPCA56546.2023.10071074.
10. K. Al-Hawaj, O. Afuye, S. Agwa, A. Apsel and C. Batten, "Towards a Reconfigurable Bit-Serial/Bit-Parallel Vector Accelerator using In-Situ Processing-In-SRAM," 2020 **IEEE International Symposium on Circuits and Systems (ISCAS)**, Seville, Spain, 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9181068.