AKSHARA VERMA, PhD

Semiconductor Research Engineer | Device Fabrication, Validation & Electrical Characterization
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Open to relocation | Fully authorized to work in the U.S.

PROFESSIONAL PROFILE

Applied Physics PhD with 10+ years of **hands-on semiconductor device fabrication**, building patterned devices end-to-end through **thin-film deposition, lithography, etch, metrology, and electrical characterization**. Intel-partnered PhD research on **top-down silicon nanowire test devices on SOI**, published as first author in **IEEE Transactions on Electron Devices**. Skilled at **connecting materials, doping, and interface quality to device performance** and feeding insights back into process development. Most recently developed **in-situ, real-time sensors for thermal process monitoring**. Currently document structured engineering knowledge for AI training as an **xAI STEM Specialist in Electrical Engineering**.

EXPERIENCE

STEM SPECIALIST – ELECTRICAL ENGINEERING | xAI | Remote *2026 – Present*

- **Engineering Knowledge for AI Training:** Create and solve advanced electrical engineering and semiconductor device problems used to train and evaluate frontier AI models.
- **Technical Evaluation & Documentation:** Assess AI-generated engineering reasoning for accuracy and rigor, and document clear, structured explanations of correct solutions.
- **Hardware & Python Projects:** Contribute hands-on hardware systems expertise and Python programming to ongoing technical projects.

PROCESS ENGINEER | MetroMapper | Fremont, CA *2023 – 2025*

- **End-to-End Device Builds:** Owned the full cleanroom workflow for in-situ, real-time sensor prototypes for semiconductor process equipment, taking designs from concept through fabrication to working hardware.
- **Thermal Process Monitoring:** Developed sensors to monitor thermal conditions during processing, delivering accurate, real-time data to equipment users to improve process yield and extend equipment lifetime.
- **Data-Driven Process Feedback:** Built Python-based data pipelines to monitor process variability and drove root-cause analysis, reducing device failure rates and feeding findings back into process development.
- **Innovation:** Contributed to early-stage IP strategy and patent filings by optimizing sensor architecture for high-performance scaling.

RESEARCH ENGINEER | Ubiquetherm | Remote/Hybrid *2020 – 2022*

- **Film-Stack Modeling:** Applied FDTD and Drude theory to model multilayer semiconductor stacks, optimizing spectral response for optical sensors.
- **Deposition & Etch Integration:** Worked with cleanroom teams to refine deposition and etch sequences, ensuring fabrication compatibility for advanced thermal materials.

PhD RESEARCHER (INTEL-PARTNERED) | CRANN, Trinity College Dublin, Ireland *2013 – 2019*

- **Patterned Test Devices:** Built silicon nanowire test devices end-to-end on doped SOI, owning the EBL (HSQ) and RIE modules, contact deposition, and electrical measurement, with widths from sub-30 nm to 500 nm.
- **Yield Improvement:** Optimized HSQ resist processes, achieving high-resolution patterning and a significant increase in device yield over previous benchmarks.
- **Custom Test Structures:** Formed intimate sidewall Hall contacts using angled evaporation with the nanowire itself as a shadow mask, and corrected for longitudinal pickup in non-opposed electrode geometries.
- **Materials-to-Device Insight:** Measured Hall mobility at 14 T in rotating magnetic fields and showed ~3× higher mobility in 40 nm nanowires than in the unpatterned SOI layer (292 vs. 100 cm^2/Vs), linking doping profile and geometry to transport.
- **Interface & Contact Analysis:** Developed an active voltage-contrast SEM method to assess electrical contact formation on single nanowires.

RESEARCH ASSISTANT | Intel-Supported Project | Dublin, Ireland *2013*

- **Industry Collaboration (Intel):** Fabricated high-resolution InAs nanowires using e-beam lithography for Intel-sponsored research.
- **Uniformity:** Tuned lithography parameters to improve material yield and device uniformity across processed wafers.

TECHNICAL SKILLS

Lithography: Photolithography (UV), electron-beam lithography (Raith, HSQ), micro-stereolithography
Thin-Film Deposition: PVD (e-beam and thermal evaporation, angled shadow evaporation), metal lift-off, dopant diffusion
Etch & Clean: RIE, ICP-RIE, plasma ashing, HF/RCA cleaning
Metrology: SEM (incl. active voltage contrast), AFM, profilometry, ellipsometry, FTIR
Electrical Characterization: Hall effect (to 14 T, rotating field), cryogenic magnetotransport, 4-point probe, in-situ thermal sensing
Device Physics & Integration: Semiconductor device physics, carrier transport, process integration, CMOS flow, FDTD and Drude modeling
Data & AI: Python, MATLAB, SQL, JMP (DOE/SPC), OriginPro; technical documentation and evaluation for AI training

SELECTED PUBLICATIONS

1. **A. Verma**, K. Borisov, S. Connaughton, P. Stamenov, “Hall effect measurements in rotating magnetic field on sub-30-nm silicon nanowires fabricated by a top–down approach,” *IEEE Transactions on Electron Devices*, 67(11), 5201–5208 (2020).
2. **A. Verma**, S. Connaughton, P. Stamenov, “Multiple contacts investigation of single silicon nanowires with the active voltage contrast scanning electron microscopy technique,” *Measurement Science and Technology*, 30, 017002 (2019).
3. T. Krishnamoorthy, M. Z. Tang, **A. Verma**, A. S. Nair, D. Pliszka, S. G. Mhaisalkar, S. Ramakrishna, “A facile route to vertically aligned electrospun SnO_2 nanowires on a transparent conducting oxide substrate for dye-sensitized solar cells,” *Journal of Materials Chemistry*, 22(5), 2166–2172 (2012).
4. T. Krishnamoorthy, V. Thavasi, **V. Akshara**, A. S. Kumar, D. Pliszka, S. G. Mhaisalkar, S. Ramakrishna, “Direct deposition of micron-thick aligned ceramic TiO_2 nanofibrous film on FTOs by double-needle electrospinning using air-turbulence shielded disc collector,” *Journal of Nanomaterials*, 2011, 739241 (2011).

EDUCATION & CERTIFICATIONS

PhD, Applied Physics | School of Physics, Trinity College Dublin, Ireland
M.Tech, Nanotechnology | Amity University, India
B.Tech, Electronics and Communications | Dr. A.P.J. Abdul Kalam Technical University, India
Microchip Fabrication Course | UCSB (2025): refresher on full CMOS flow, oxidation, and diffusion
Lean Six Sigma Green Belt | In progress

AWARDS & SCHOLARSHIPS

Irish Research Council Enterprise Partnership Scholarship (with Intel) | Trinity College Dublin (2013–2016)
Science Foundation Ireland (SFI) Postgraduate Scholarship | Trinity College Dublin (2016–2018)
Teaching Assistantship Award | School of Physics, Trinity College Dublin (2014–2015)